Digital Systems and Microprocessors

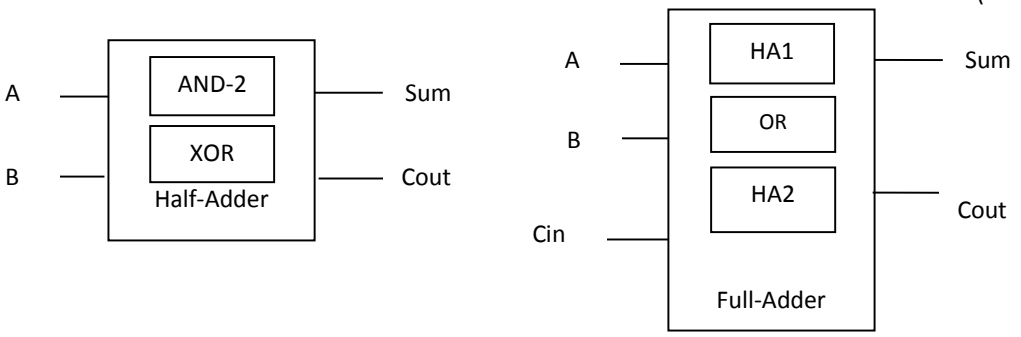
Lab Assignment-3

Assignment Date: Thursday, 26th October 2017
Maximum Marks: 20
Due Date: Monday: 6th Nov 2017

Pre-requisites:

1. Learn basic combinational logic blocks
2. Learn how to create and use a User Constraints File (hint: They are different for different boards)

Q1. (a) First create modules for AND and XOR gates using **behavioral modeling** scheme.
(b) Use these modules to implement a Half-Adder using **structural modeling** .
(c) Using the Half-Adder design and OR gate module, implement a Full-Adder design using **structural modeling**. Write a testbench and simulate your Full Adder design.
(4 marks)



Q2. Using the Full-Adder design in Ques 1(c), construct a 4-bit ripple carry adder using **structural modeling**. Write a testbench to simulate your design. (4 marks)

Q3. Using **Gate-Level primitives** implement a Full-Subtractor design. Simulate and test your design using testbench. (4 marks)

Q4. Design a 4-bit Adder-Subtractor module using **structural modeling**. Simulate your design using testbench. (5 marks)

Q5. Write a User Constraints File file for Questions 1 and 3. Map the input and output (I/O) ports of your design to I/O interfaces on the FPGA board. The I/O interfaces of the Zybo FPGA board can be obtained from the documentation provided on Blackboard. Generate the bitstream file. Use the bitstream file to download your design on a Zybo FPGA board and run it on the FPGA itself. (3 marks)